Abstract

The current invention provides a system and method for maintaining memory coherency within a multiprocessor environment that includes multiple requesters such as instruction processors coupled to a shared main memory. Within the system of the current invention, data may be provided from the shared memory to a requester for update purposes before all other read-only copies of this data stored elsewhere within the system have been invalidated. To ensure that this acceleration mechanism does not result in memory incoherency, an instruction is provided for inclusion within the instruction set of the processor. Execution of this instruction causes the executing processor to discontinue execution until all outstanding invalidation activities have completed for any data that has been retrieved and updated by the processor.